In the Claims:

Please amend claims 18, 19, 26, 48, 49 and 56. Please cancel claims 24 and 54. Please add new claims 61 and 62. The claims are as follows:

1 - 17 (Canceled)

18. (Currently Amended) A semiconductor device with improved leakage control, comprising:

a P doped semiconductor substrate having a top surface;

a STI in said substrate, said STI having a bottom, a first sidewall and an opposite second sidewall;

a P-type leakage stop implant in said substrate under the bottom of said STI, all of said P-type leakage stop implant ~~and under and~~ aligned [[to]] between said second sidewall and an axis equally spaced between said first and second sidewalls; and

an N-well in said substrate adjacent to and in contact with said first sidewall, said N-well extending under said STI and forming an upper side portion of an isolation junction with said leakage stop implant and forming a bottom and a lower side portion of said junction with dopant species in said substrate, said upper portion of said isolation junction located entirely under said STI.

19. (Currently Amended) The semiconductor device of claim 18, further comprising a P-well in said substrate adjacent to and in contact with said second sidewall, said P-well incorporated into said ~~upper portion and forming a lower portion of said~~ isolation junction ~~with said N-well~~.

20. (Original) The semiconductor device of claim 18, wherein said leakage stop implant extends under said STI from said second sidewall toward said first sidewall a distance equal to 10 to 40% of the width of said STI

21. (Original) The semiconductor device of claim 18, wherein the concentration of P dopant at an interface formed by the bottom of said STI and said substrate is 3E16 atm/cm^3 to 1E17 atm/cm^3.

22. (Original) The semiconductor device of claim 21, wherein the concentration of P dopant at about 0.1 micron below said interface under said second sidewall is 1.0E17 atm/cm^3 to 1.5E17 atm/cm^3.

23. (Original) The semiconductor device of claim 18, further comprising spacers on said first and second sidewalls of and contained within said STI.

24. (Canceled)

25. (Original) The semiconductor device of claim 18, wherein said STI is filled with TEOS or HDP oxide.

26. (Currently Amended) The semiconductor device of claim 25, further including a liner on said bottom, said first sidewall and said second sidewall of said STI.

27. (Original) The semiconductor device of claim 26, wherein said liner is 10 to 30 nm thick thermal oxide.

28. (Original) The semiconductor device of claim 26, further comprising spacers on said liner over said first and second sidewalls of and contained within said STI

29. (Original) The semiconductor device of claim 19, wherein said STI is 0.05 to 1 micron in depth and 0.1 to 5 microns in width.

30. (Original) The semiconductor device of claim 19, further comprising a PFET in said N-well and an NFET in said P-well.

31-47 (Canceled)

48. (Original) (Currently Amended) A semiconductor device with improved leakage control, comprising:

an N doped semiconductor substrate having a top surface;

a STI in said substrate, said STI having a bottom, a first sidewall and an opposite second sidewall;

an N-type leakage stop implant in said substrate under the bottom of said STI, all of said P-type leakage stop implant ~~and under~~ and aligned [[to]] between said second sidewall and an axis equally spaced between said first and second sidewalls; and

a P-well in said substrate adjacent to and in contact with said first sidewall, said P-well extending under said STI and forming an upper side portion of an isolation junction with said leakage stop implant and forming a bottom and a lower side portion of said junction with dopant species in said substrate, said upper portion of said isolation junction located entirely under said STI.

49. (Currently Amended) The semiconductor device of claim 48, further comprising an N-well in said substrate adjacent to and in contact with said second sidewall, said N-well incorporated into ~~said upper portion and forming a lower portion of~~ said isolation junction ~~with said~~ P-well.

50. (Original) The semiconductor device of claim 48, wherein said leakage stop implant extends under said STI from said second sidewall toward said first sidewall a distance equal to 10 to 40% of the width of said STI

51. (Original) The semiconductor device of claim 48, wherein the concentration of N dopant at an interface formed by the bottom of said STI and said substrate is 3E16 atm/cm^3 to 1E17 atm/cm^3.

52. (Original) The semiconductor device of claim 51, wherein the concentration of N dopant at about 0.1 micron below said interface under said second sidewall is 1.0E17 atm/cm^3 to 1.5E17 atm/cm^3.

53. (Original) The semiconductor device of claim 48, further comprising spacers on said first and second sidewalls of and contained within said STI.

54. (Canceled)

55. (Original) The semiconductor device of claim 48, wherein said STI is filled with TEOS or HDP oxide.

56. (Currently Amended) The semiconductor device of claim 55, further including a liner on said bottom, said first sidewall and said second sidewall of said STI.

57. (Original) The semiconductor device of claim 56, wherein said liner is 10 to 30 nm thick thermal oxide.

58. (Original) The semiconductor device of claim 56, further comprising spacers on said liner over said first and second sidewalls of and contained within said STI

59. (Original) The semiconductor device of claim 49, wherein said STI is 0.05 to 1 micron in depth and 0.1 to 5 microns in width.

60. (Original) The semiconductor device of claim 49, further comprising an NFET in said P-well and a PFET in said N-well.

61. (New) The semiconductor device of claim 18, wherein:

said isolation junction contacts said bottom of said STI a first distance from said second sidewall of said isolation junction;

said isolation junction extends from said second sidewall a second distance at a first depth below said bottom of said STI;

said isolation junction extends from said second sidewall a third distance at a second depth below said bottom of said STI;

said isolation junction extends from said second sidewall a fourth distance at a third depth below said bottom of said STI;

said first depth less than said second depth, said second depth less than said third depth; and

said first and third distances greater than said second distance and first, second and third distances greater than said fourth distance.

62. (New) The semiconductor device of claim 48, wherein:

said isolation junction contacts said bottom of said STI a first distance from said second sidewall of said isolation junction;

said isolation junction extends from said second sidewall a second distance at a first depth below said bottom of said STI;

said isolation junction extends from said second sidewall a third distance at a second depth below said bottom of said STI;

said isolation junction extends from said second sidewall a fourth distance at a third depth below said bottom of said STI;

said first depth less than said second depth, said second depth less than said third depth; and

said first and third distances greater than said second distance and first, second and third distances greater than said fourth distance.